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L9: (1) "6331943".PN. | US 6331943 B1 | Tag: S | Doc: 1/1

	Document ID	Kind Codes	Source	Issue Date	Pa
1	US 6331943 B1		USPAT	20011218	17

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(12) United States Patent
Naji et al.

(10) Patent No.: US 6,331,943 B1
(45) Date of Patent: Dec. 18, 2001

(54) **MTJ MRAM SERIES-PARALLEL ARCHITECTURE**

(75) Inventors: Peter K. Naji, Phoenix; Mark DeHerrera, Tempe; Mark Durlam, Chandler, all of AZ (US)

(73) Assignee: Motorola, Inc., Schaumburg, IL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/649,117

(22) Filed: Aug. 28, 2000

(51) Int. Cl.[7] G11C 11/00

(52) U.S. Cl. 365/158; 365/171

(58) Field of Search 365/158, 171, 365/173

(56) References Cited

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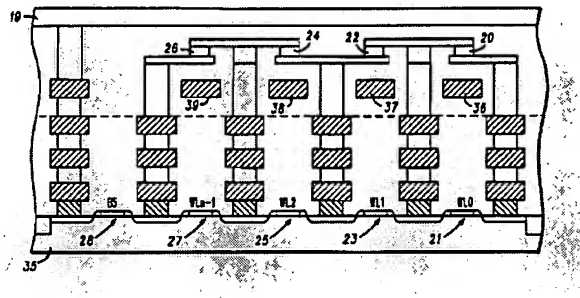
Primary Examiner—Son T. Dinh
(74) *Attorney, Agent, or Firm*—William E. Koch

(57) **ABSTRACT**

Magnetic tunnel junction random access memory architecture in which an array of memory cells is arranged in rows and columns and each memory cell includes a magnetic tunnel junction and a control transistor connected in parallel. A control line is connected to the gate of each control transistor in a row of control transistors and a metal programming line extending adjacent to each magnetic tunnel junction is connected to the control line in spaced apart intervals by vias. Further, groups of memory cells in each column are connected in series to form local bit lines which are connected in parallel to global bit lines. The series-parallel configuration is read using a centrally located column to provide a reference signal and data from columns on each side of the reference column is compared to the reference signal or two columns in proximity are differentially compared.

23 Claims, 9 Drawing Sheets



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L10: (1) "6324093".PN. | US 6324093 | Tag: S | Doc: 1/1 | "Full" 1/14 (Total images 14)

US006324093B1

(12) **United States Patent**
Perner et al.

(10) Patent No.: **US 6,324,093 B1**
(45) Date of Patent: **Nov. 27, 2001**

(54) WRITE-ONCE THIN-FILM MEMORY

(75) Inventors: Frederick A. Perner, Palo Alto; Thomas C. Anthony, Sunnyvale, both of CA (US)

(73) Assignee: Hewlett-Packard Company, Palo Alto, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/663,016

(22) Filed: Sep. 15, 2000

(51) Int. Cl.^{7} G11C 11/14

(52) U.S. Cl. 365/171; 365/53; 365/56

(58) Field of Search 365/171, 55, 66, 365/52, 63, 129

(56) References Cited

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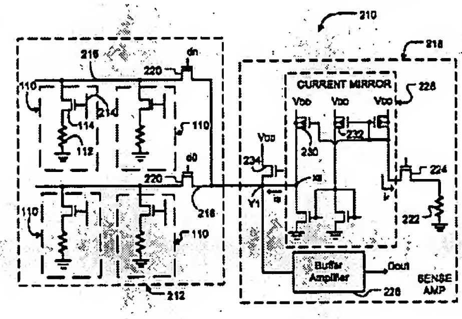
Primary Examiner—Hoai V. Ho

(57) ABSTRACT

A data storage device includes a group of memory cells. Write-once operations may be performed by damaging the thin-film barriers of at least some of the memory cells. The data storage device may be a Magnetic Random Access Memory ("MRAM") device.

25 Claims, 7 Drawing Sheets



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L3: (8) 2 and progra... | US 6683807 B2 | Tag: S | Doc: 5/8

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1	US 20030090935		US-PGPU	20030515	48
2	US 20030007598		US-PGPU	20030109	78
3	US 20020184539		US-PGPU	20021205	44
4	US 20020006222		US-PGPU	20020117	31
5	US 6683807 B2		USPAT	20040127	46
6	US 5041924 A		USPAT	19910820	73
7	US 4445776 A		USPAT	19840501	75
8	US 4120583 A		USPAT	19781017	75

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L3: (8) 2 and progra... | US 6683807 | Tag: S | Doc: 5/8 | "Full" 1/46 (Total images 46)

US006683807B2

(12) **United States Patent**
Hidaka

(10) Patent No.: **US 6,683,807 B2**
(45) Date of Patent: **Jan. 27, 2004**

(54) **THIN FILM MAGNETIC MEMORY DEVICE FOR PROGRAMMING REQUIRED INFORMATION WITH AN ELEMENT SIMILAR TO A MEMORY CELL AND INFORMATION PROGRAMMING METHOD**

(75) Inventor: Hideto Hidaka, Hyogo (JP)

(73) Assignee: Mitsubishi Denki Kabushiki Kaisha, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 10/234,343

(22) Filed: Sep. 5, 2002

(65) Prior Publication Data

US 2003/0090935 A1 May 15, 2003

(30) Foreign Application Priority Data

Nov. 14, 2001 (JP) 2001-348800
Mar. 13, 2002 (JP) 2002-070268

(51) Int. Cl.[7] G11C 11/14

(52) U.S. Cl. 365/158; 365/232; 365/243.5

(58) Field of Search 365/158, 55, 66, 74, 87, 97, 230, 240.5

(56) References Cited

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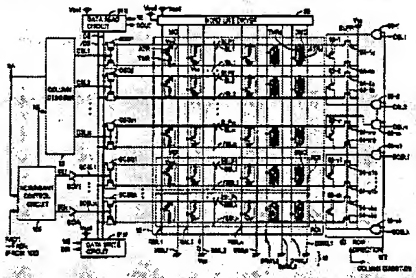
Primary Examiner—Thong Le
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) **ABSTRACT**

A program unit includes two program cells having an electric resistance varying according to a magnetization direction thereof. These program cells are magnetized in the same direction in initial state, that is, non-program state. In program state, the magnetization direction of one of the program cells selected according to program data is changed from the initial state. One-bit program data and information of whether the program unit stores program data or not can be read based on two program signals generated according to the electric resistances of the two program cells.

19 Claims, 26 Drawing Sheets



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